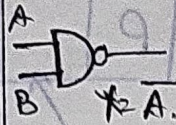
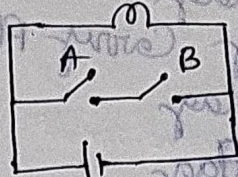
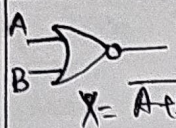
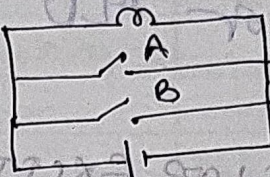
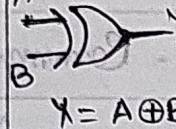
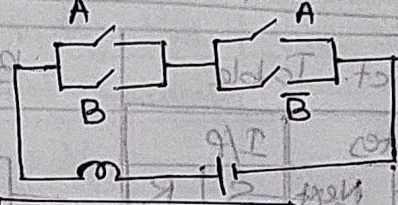
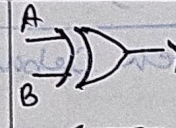
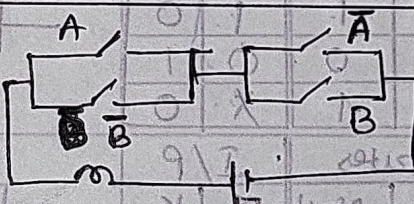
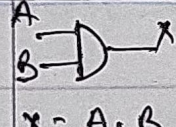
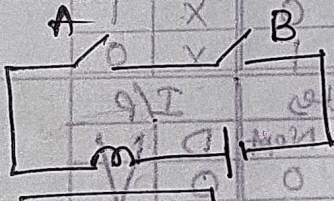
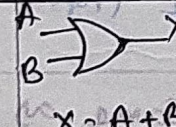
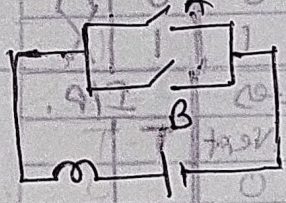
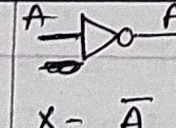
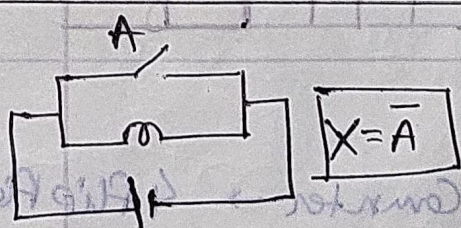
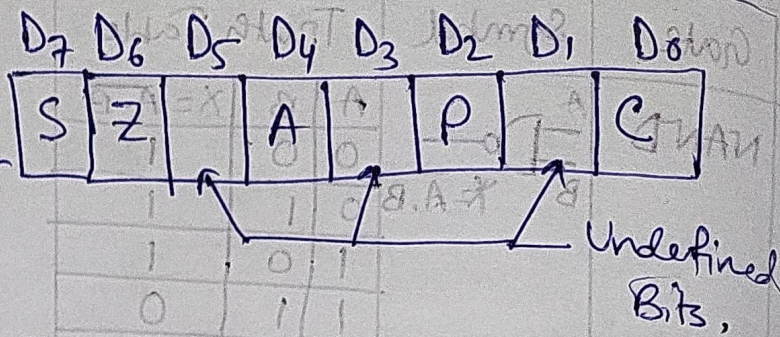


Sl. No.	Gate	Symbol	Truth Table	Eqv. Circuit.	IC No.															
1.	NAND	 $X = A \cdot B$	<table><tr><th>A</th><th>B</th><th>$X = A \cdot B$</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	$X = A \cdot B$	0	0	1	0	1	1	1	0	1	1	1	0	 $X = A \cdot B$	7400 (Series)
A	B	$X = A \cdot B$																		
0	0	1																		
0	1	1																		
1	0	1																		
1	1	0																		
2.	NOR	 $X = A + B$	<table><tr><th>A</th><th>B</th><th>$X = A + B$</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	$X = A + B$	0	0	1	0	1	0	1	0	0	1	1	0	 $X = A + B$	7402 (Parallel)
A	B	$X = A + B$																		
0	0	1																		
0	1	0																		
1	0	0																		
1	1	0																		
3.	XOR	 $X = A \oplus B$	<table><tr><th>A</th><th>B</th><th>$X = A \oplus B$</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	$X = A \oplus B$	0	0	0	0	1	1	1	0	1	1	1	0	 $X = \bar{A}B + A\bar{B}$	7484 (Half Adder)
A	B	$X = A \oplus B$																		
0	0	0																		
0	1	1																		
1	0	1																		
1	1	0																		
4.	XNOR	 $X = A \odot B$	<table><tr><th>A</th><th>B</th><th>$X = A \odot B$</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	$X = A \odot B$	0	0	1	0	1	0	1	0	0	1	1	1	 $X = AB + \bar{A}\bar{B}$	
A	B	$X = A \odot B$																		
0	0	1																		
0	1	0																		
1	0	0																		
1	1	1																		
5.	AND	 $X = A \cdot B$	<table><tr><th>A</th><th>B</th><th>$A \cdot B$</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	$A \cdot B$	0	0	0	0	1	0	1	0	0	1	1	1	 $X = A \cdot B$	7408 (Series)
A	B	$A \cdot B$																		
0	0	0																		
0	1	0																		
1	0	0																		
1	1	1																		
6.	OR	 $X = A + B$	<table><tr><th>A</th><th>B</th><th>$A + B$</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	$A + B$	0	0	0	0	1	1	1	0	1	1	1	1	 $X = A + B$	7432 (Parallel)
A	B	$A + B$																		
0	0	0																		
0	1	1																		
1	0	1																		
1	1	1																		
7.	NOT	 $X = \bar{A}$	<table><tr><th>A</th><th>$\bar{A}$</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	A	$\bar{A}$	0	1	1	0	 $X = \bar{A}$	7404									
A	$\bar{A}$																			
0	1																			
1	0																			

8085 MP Flags.

Bit Position of Flag Register

- S = Sign Flag
- Z = Zero Flag
- A = Auxiliary Carry Flag
- P = Parity Flag
- C = Carry Flag



MP Consists of ALU

ElectricalNoteBook.com

FLIP-FLOP EXCITATION TABLE

A Bistable Multivibrator, Comments,

S.No.	Flip-Flop	Exct. Table	Block Diagram	Comments																								
1.	S-R FF (Set/Reset)	<table border="1"> <thead> <tr> <th colspan="2">States</th> <th colspan="2">I/P</th> </tr> <tr> <th>Prev.</th> <th>Next</th> <th>S</th> <th>R</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>X</td> <td>0</td> </tr> </tbody> </table>	States		I/P		Prev.	Next	S	R	0	0	0	X	0	1	1	0	1	0	0	1	1	1	X	0		Chang eqⁿ $Q(t+1) = S + Q\bar{R}$ Switch Debouncer.
States		I/P																										
Prev.	Next	S	R																									
0	0	0	X																									
0	1	1	0																									
1	0	0	1																									
1	1	X	0																									
2.	JK FF	<table border="1"> <thead> <tr> <th colspan="2">States</th> <th colspan="2">I/P</th> </tr> <tr> <th>Prev.</th> <th>Next</th> <th>J</th> <th>K</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>X</td> </tr> <tr> <td>1</td> <td>0</td> <td>X</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>X</td> <td>0</td> </tr> </tbody> </table>	States		I/P		Prev.	Next	J	K	0	0	0	X	0	1	1	X	1	0	X	1	1	1	X	0		Race Around Condition $Q(t+1) = \bar{Q}J + Q\bar{K}$
States		I/P																										
Prev.	Next	J	K																									
0	0	0	X																									
0	1	1	X																									
1	0	X	1																									
1	1	X	0																									
3.	D type F/R (Delay)	<table border="1"> <thead> <tr> <th colspan="2">States</th> <th>I/P</th> </tr> <tr> <th>Prev.</th> <th>Next</th> <th>D</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	States		I/P	Prev.	Next	D	0	0	0	0	1	1	1	0	0	1	1	1		$Q(t+1) = D$ One inp.						
States		I/P																										
Prev.	Next	D																										
0	0	0																										
0	1	1																										
1	0	0																										
1	1	1																										
4.	T type P/F. (Toggle)	<table border="1"> <thead> <tr> <th colspan="2">States</th> <th>I/P</th> </tr> <tr> <th>Prev.</th> <th>Next</th> <th>T</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	States		I/P	Prev.	Next	T	0	0	0	0	1	1	1	0	1	1	1	0		⊗ Same as XOR gate						
States		I/P																										
Prev.	Next	T																										
0	0	0																										
0	1	1																										
1	0	1																										
1	1	0																										

ElectricalNotebook.com

Decade Counter → 4 Flip Flop.

Combinational Ckt faster than Sequential Ckt. (Latch, F/F)

Clocked Unclocked

P/F → Sequential Edge

ElectricalNoteBook.com

Resolution of ADC $\Rightarrow 2^n$ ($n = \text{no. of bit}$)

Min No. of bit required $= \frac{\text{Voltage}}{\text{Resolution}}$

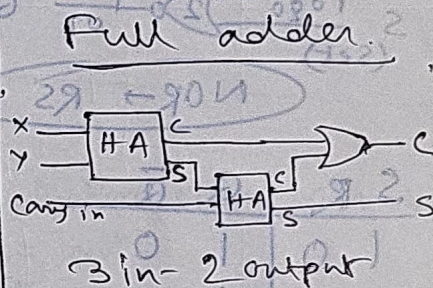
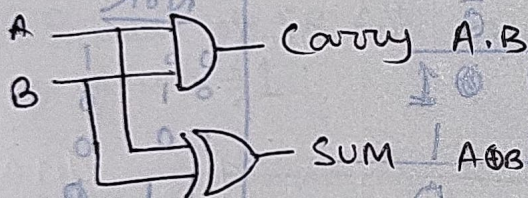
7 OSI model layers. ElectricalNotebook.com

TCP/IP Model

Host Layer	Application	Data Generation	Data	Application
7	Application	Data Generation	Data	Application
6	Presentation	Encryption & Formatting	Data	Application
5	Session	Establish connection	Data	Application
4	Transport	Delivery & sequencing	Segment	Transport
3	Network	Routing to destination	Packets	Internet
2	Data Link	Local N/w Host Delivery	Frames	N/w
1	Physical	Access to Media	Bits	Access

Satellite communication through Transponder.

Half Adder $\rightarrow$ AND + X-OR Gate.



ElectricalNotebook.com

Flip Flop has 2 stable state $\rightarrow$ off are complementary.

Fastest Logic $\rightarrow$ Emitter Coupled Logic (ECL)

Decade Counter $\rightarrow$ 4 f.f.

Schmitt Trigger

Bi-stable Multivibrator (latch or f.f.)

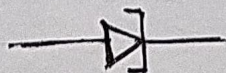
(i) Application $\rightarrow$ A/D Converter, level detection,

(ii) Comparator ckt. with hysteresis

(iii) +ve f.b. to form ~~inverting~~ inverting i/p of a Comparator or. differ. amp.

(iv) Square wave generation.

Tunnel Diode



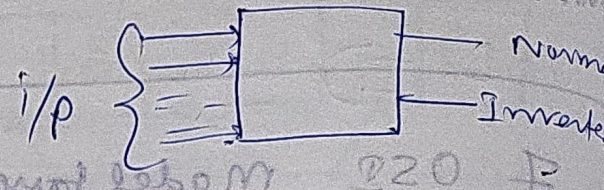
(i) -ve Resistance Region.

(ii) Other name $\rightarrow$ Esaki Diode.

(iii) Heavily doped pn junction.

Flip Flops:-

- Can store 1 bit info.
- Used in closed sequential ckt.
- Has 2 o/p.
- Normal
- Complement.



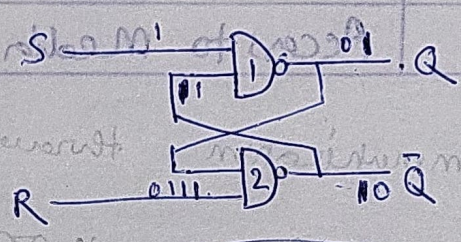
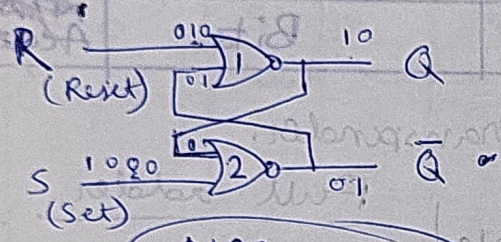
Bi-stable Multivibrator. — 2 stable state

- SR, JK, D, T

Basic P/P. or Latch

Latch → Asynchronous
Unlocked F/F

2 NAND gate or 2 NOR gate



NOR → RS

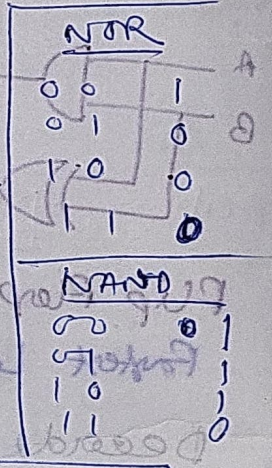
NAND → SR

S	R	Q	Q̄
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

Invalid.
(Don't Care)

S	R	Q	Q̄
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	1	1

Invalid
(Don't Care)

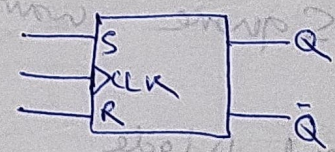
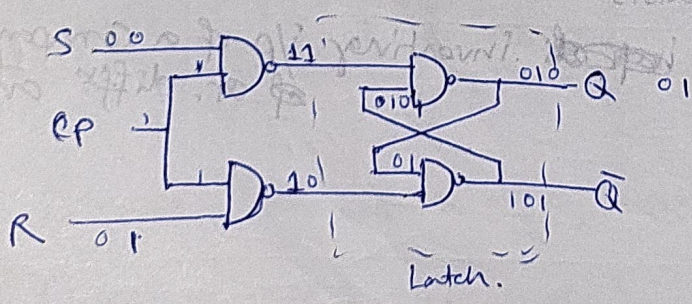


Unlocked → Asynch.
Clocked → Synch.

Latch consist of 2 inverters

Clocked SR F/F. (CLK pin)

Latch → NOR
CP → AND gate.



Characteristic Table

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Q = Present
Q(t+1) = Next

Present i/p.
Next o/p.

Characteristic Table

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X (both Q, $\bar{Q}$ = 1)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

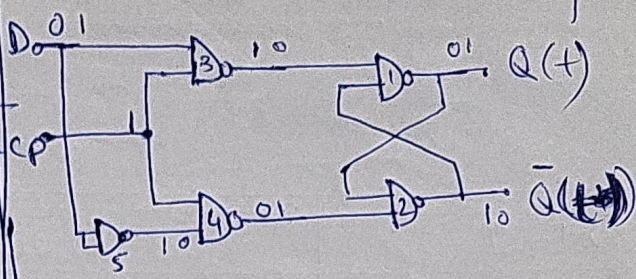
S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	X

D - F/F (Delays)

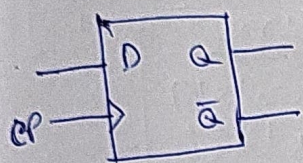
Modification of SR clocked F/F.

WAND

00	1
01	1
10	1
11	0



ElectricalNoteBook.com



Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Q(t)	$\bar{D}$	D
0	1	1
1	0	0

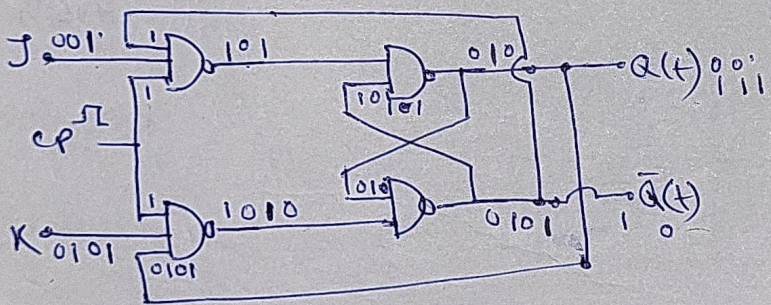
$$Q(t+1) = D$$

D	Q(t+1)
0	0
1	1

J-K F/F

ElectricalNotebook.com

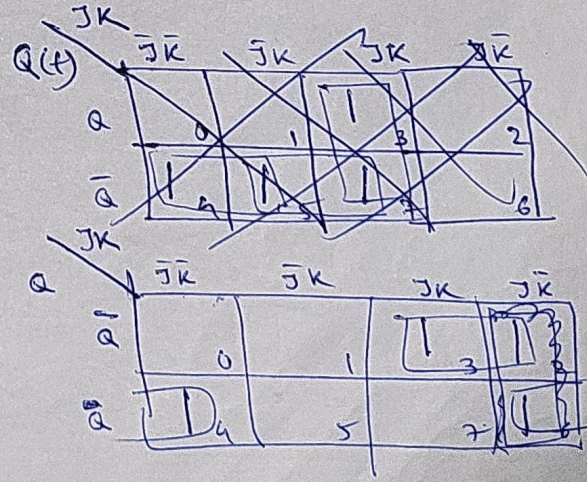
Refinement of SR F/F. to solve problem of indetermination state when both i/p are $\Rightarrow 1$.



Q(t)	Set	Reset	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1 (Comp of Q(t))
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0 (Comp of Q(t))

Set $\Rightarrow 1$
Reset $\Rightarrow 0$

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

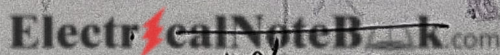


Race Around Condition $\rightarrow$ JK

- 4 Stable state $\rightarrow$
- ① Latch
 - ② Reset
 - ③ Set
 - ④ Toggle

$$Q(t+1) = Q(t)J + \bar{J}K + Q(t)\bar{K}$$

ElectricalNoteBook.com



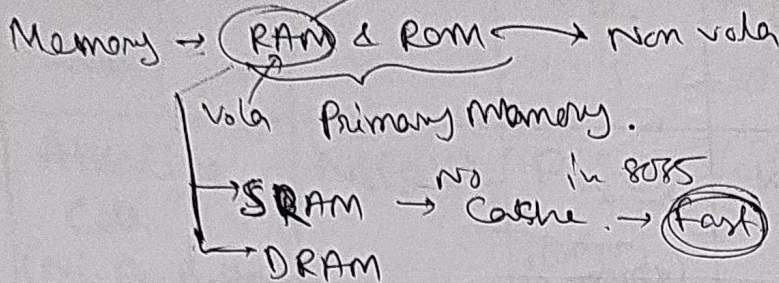
Basic of MP.

Intel - 8085
8086
80186
286
386
486

80586 - P1, P2, P3, P4 - C2D, Core i7.
Core 2 Duo.

Pentium 1

MP. use.



ElectricalNotebook.com

Pixel
Picture element.

SRAM stores data in flip flop. (Faster)
DRAM " " " Capacitor. (slower) charging & discharging

- Fetch an instruction, from memory.
- Decode (understanding 'opcode')
every inst. has different 'opcode'
- Execute

ElectricalNoteBook.com

$a = b + c$; HLL
ADD B, C; ASM
0110011 ← LLL/MK/Ob/...
"opcode" Machine Code

Bin & Hexa

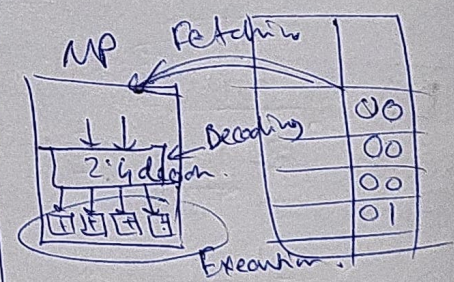
0000 0001 1001	Dec. 0 1 9	Hex 0H 1H 9H AH BH CH DH EH FH	Bin. 0011 1001 1010 35H → 0011 0101 74H → 0111 0100 FFH → 1111 1111
----------------------	---------------------	---	---

8 bit → Byte
00H → 0000 0000
FFH → 1111 1111 → 8 bit.
5136 H → 0101 0001 0011 0110 → 16 bit.

16 bit → Word

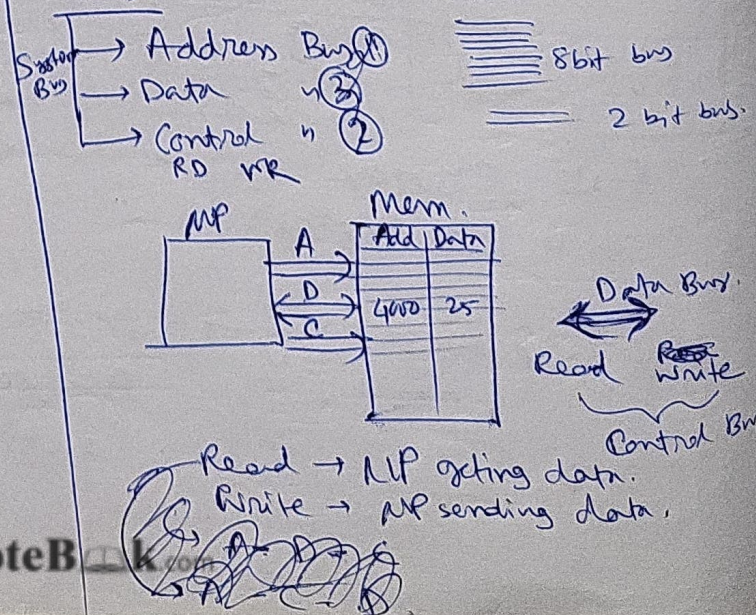
M/C	ASM
00	ADD
01	SUB
10	MUL
11	DIV

Memory



$2^0 = 1$
 $2^1 = 2$
 $2^2 = 4$
 $2^{10} = 1K$
 $2^{11} = 2^1 \times 2^{10} = 2K$
 $2^{12} = 4K$
 $2^{13} = 8K$
 $2^{14} = 16K$
 $2^{15} = 32K$
 $2^{20} = 1M [1K \times 1K]$
 $2^{30} = 1G [1M \times 1M]$
 $2^{40} = 1T$
 $4GB = 2^2 \times 2^{30} = 2^{32}$
 $256GB = 2^8 \times 2^{30} = 2^{38}$

Bus.



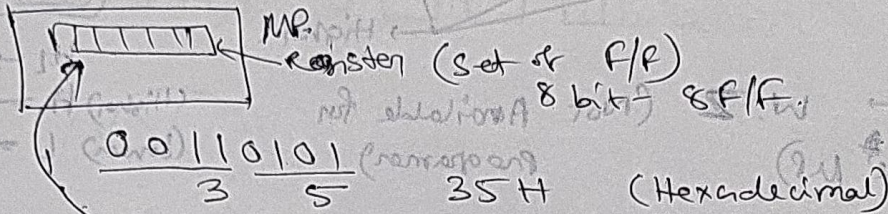
ElectricalNoteBook.com

Register:-

- 6 general purpose Register. B, C, D, E, H, L (8 bit data store)
- 2 internal n W, Z (CALL, XCHG inst.)
- 2 16-bit P.C., 16 bit S.P.
- 1 increment/decrement counter & register.
- 1 Multiplexer (mux)
- Register pair $\rightarrow$ BC, DE, HL. (perform 16 bit operation)
- Store (Money bag)

ElectricalNotebook.com

Fetching
Decoding
Execution.



General Purpose Register (To store value)

⊕ Assemble Level Language. (Variable $\rightarrow$ Register).

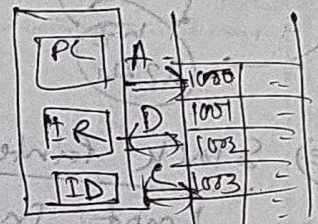
Software $\rightarrow$ Hardware

$\Rightarrow$ 7, 8 bit General Purpose Register.
(B, C, D, E, H, L, A).

Special Purpose Register

PC $\rightarrow$ Address of next instruction.

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IR: Inst. Register
ID: n Decoder

$\Rightarrow$ In 8085 1st operand is to be stored in register A (Accumulator) by default.

$\Rightarrow$ and result will be stored in A.

ADD B $\rightarrow$ A + B $\rightarrow$ A
ADD C $\rightarrow$ A + C $\rightarrow$ A
ADD D $\rightarrow$ A + D $\rightarrow$ A

Accumulator.

(16) A₂ Address bus
(8) D = Data $\sim$
(2) Control $\sim$

ADD B $\rightarrow$ Inst. stored in memory.

- ① Address from PC.
- ② Instruction stored in address.
- ③ Address bus (20 bits) Address bus (20 bits) memory @ 2000
- ④ Processor Read 2000.
- ⑤ Data bus (8 bits) Instruction 2000
- ⑥ 8 bit internal data bus (8 bits)
- ⑦ Inst. register. (Fetching Complete)
- ⑧ Inst. decode $\rightarrow$ timing & control.
- ⑨ T & C Unit Accumulator $\rightarrow$ 2000 value
- ⑩ 2nd signal select B Register $\rightarrow$ transfer Reg. select.
- ⑪ Multiplexer $\rightarrow$ combine 2000.
- ⑫ B 20 value Bus $\rightarrow$ 2000 Transfer Register $\rightarrow$
- ⑬ T & C ALU $\rightarrow$ 2000 Add 2000.
- ⑭ Value into Bus $\rightarrow$ 2000 T & C Unit A. 2000 value
- ⑮ Inst. complete
- ⑯ Side by side PC

ElectricalNotebook.com

Temp Register → To hold ~~data~~ ^{current} 2nd operand temporarily.

Flag Register → Tell ~~status~~ ^{status} of ~~current~~ ^{current} Result

Result → A.
Status → Flag

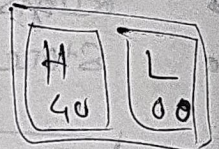
Sign Flag → true or false

Carry n → Carry over

Zero n → Result zero

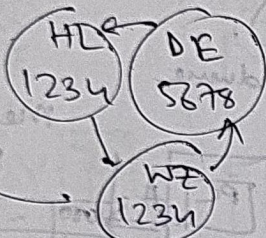
Parity n → n Even Parity odd

⇒ 16 Bit value ~~memory~~ ^{Register} use 2 pairs 20, 21, 22, 23 Register Pair. - BC, DE, HL



⇒ Temp. Register Pair → W. Z (Not Available for Programmer) (only for use MP)

XCHG



(HL & DE SP pairs interchange 20)

(exchange)

⇒ Stack Pointer

Last In First Out

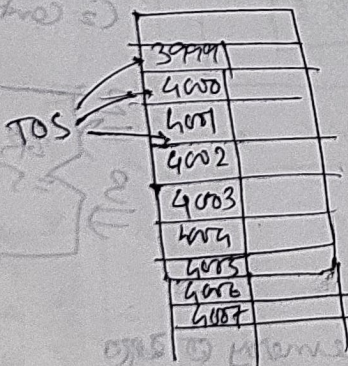
Add or Top of Stack

Operation Push

add element ~~to~~ ^{to} stack

Pop.

element ~~to~~ ^{to} register



data stack grows easily access top and

1st address (top) 3rd address (bottom)

Value of Add of

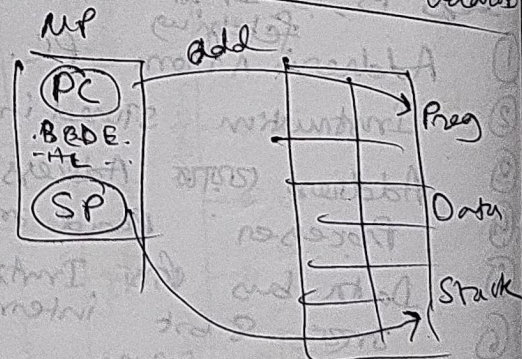
Top of Stack = 04
Top of Stack = 4002

SP = 4002

Queue Stack
(1234) (1234)
(1234) (4321)

→ address

→ top address



- ⊗ On every Push SP get decremented.
- ⊗ On n Pop SP get increment.

Pre/Dec. Address Latch. → PC 2 bits then

→ BP - incr while Pop

→ SP - dec while Push

Voltage gain in non-inv. amp.

$$\frac{V_{out}}{V_{in}} = \frac{R_2 + R_f}{R_i}$$

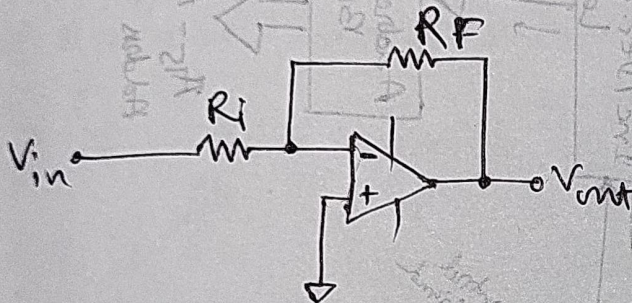
$$A_v = \frac{R_i + R_f}{R_i}$$

R_i = Input Resistor.
 R_f = Feedback Resistor

Voltage gain in Inv. amp.

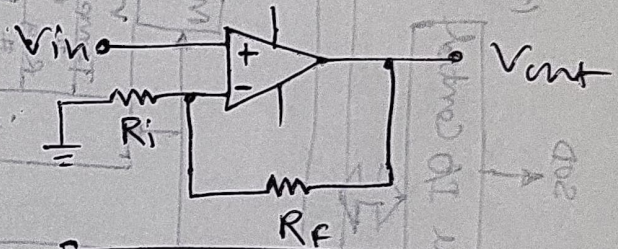
$$A_v = (-) \frac{R_f}{R_i}$$

Inverting Amp.



$$A_v = - \frac{R_f}{R_i}$$

Non-inv. Amp.



$$A_v = 1 + \frac{R_f}{R_i}$$

Input $\rightarrow$ (-)

Input $\rightarrow$ (+)

BATTERY

ElectricalNoteBook.com

Components.

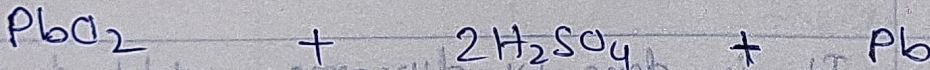
Components	Material
1. Container	Hard Rubber / Bituminous Compound
2. Plate	+ve $\rightarrow$ PbO_2 -ve $\rightarrow$ Spongy Lead
3. Separators	Rubber, Celluloided & PVC wood.
4. Cell Covers	Hard Moulded Rubber.
5. Vent Plug	PVC
6. Cell Connectors	Pure Lead
7. Partition Walls	Hard Rubber.
8. Battery Post	Pure Lead
9. Electrolyte	Dil. H_2SO_4 (at 1260 SpG)

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at fully charged condition SpG. is 1280 to 1300

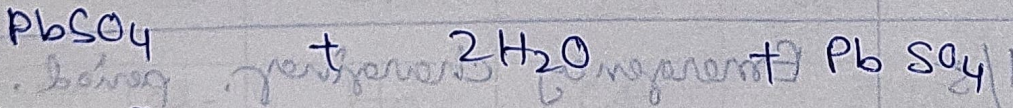
Charged $\rightarrow$

+ve Plate Electrolyte -ve Plate



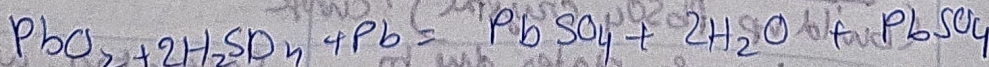
Discharged $\rightarrow$

+ve Plate Electrolyte -ve Plate



Factor affecting capacity of the battery

1. No. of plates
2. Type of electrolyte
3. Age
4. Temp.
5. Rate of discharge



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7 types of Battery charging

1. BOOSTER charging $\rightarrow \frac{1}{5}$ th capacity of battery
2. Partial $\rightarrow \frac{1}{10}$
3. Normal $\rightarrow \frac{1}{10}$
4. Refresher $\rightarrow \frac{1}{20}$
5. Initial $\rightarrow \frac{1}{30}$
6. Trickle $\rightarrow \frac{1}{50}$
7. Taper $\rightarrow$ According to dynamo rating.

Boost charging $\rightarrow$ Over discharged Battery.

Sl. No.	Charging	Charging Rate	Use
1.	Initial	$1/30$	New battery received for 1st charge
2.	Normal	$1/10$	It is given to run down bty.
3.	Refresher	$1/20$	It is given to storage bty.
4.	Trickle	$1/50$	It is given to sulphated bty.
5.	Taper		It is done by dynamo which is in vehicle. No constant charging rate
6.	Partial	$1/10$	It is given to single cell
7.	Booster	$1/5$	Emergency charging. period.

Defect in Battery

Problems.

Remedies

① Polarisation (Primary)	Collection of H_2 gas around +ve plate electrode of cell.	Use a depolarizer MnO_2 which convert H_2 bubble into water.
② Sulphation	When the L.A. battery is deprived of full charge (build up $PbSO_4$ crystal)	Periodic charge 14-16 hr.
③ Buckling	Bending of plates due to aging, sulphation etc.	Separator, use.
④ Local Action (Primary)	Presence of impurities on zinc plate. Rod	Amalgamating the Zn Rod (bathing with H_2)

Lechance cell has a depolariser

Effect of Primary cell $\rightarrow$ Local Action & Polarization.

Lechance cell $\rightarrow$ Interm. Use.

Primary Cell $\rightarrow$ Local Action ($\eta = 70\%$)
 $\rightarrow$ Polarization

Secondary Cell (L.A. Cell) $\rightarrow$ Sulphation ($\eta = 80-95\%$)
 $\rightarrow$ Bulking.

Fastest Charging Method $\rightarrow$ Const. Voltage System,
 Sedimentation $\rightarrow$ High Rate over charge

Different types of Cells. (Primary)

Sl. No.	Name	+ve	-ve	Electrolyte	EMF.
1.	Voltaic cell (*)	Cu	Zn	Dil. H_2SO_4 Depol. MnO_2	1.08 V
2.	Lechance cell	Carbon	Zn	NH_4Cl	1.4 V
3.	Dry Cell	Carbon	Zn	Paste of NH_4Cl , $ZnCl_2$, Plaster of Paris. (Depol. $\rightarrow MnO_2$)	1.5 V
4.	Daniel Cell (*)	Cu	Zn	Dil. H_2SO_4 (Depol. $\rightarrow CuSO_4$)	1.1 V
5.	Bunsen Cell	Carbon	Zn	Dil. H_2SO_4	1.95 V
6.	Werton Cadmium Cell	Hg.	Cd. Amalgam	$CdSO_4$	1.0784 V
7.	Fuel Cell	O_2 Feed (Nickel)	H_2 Feed (Nickel)	Dil. H_2SO_4 or. KOH	

Full Charge Sp. Gravity $\Rightarrow$ 1230 - 1305
 n discharge $\Rightarrow$ 1100.

For electroplating $\rightarrow$ Material to be coated $\rightarrow$ -ve
 Object.

Charging Sp. Gr. $\uparrow$
 Disn Sp. Gr. $\downarrow$

Coating Object $\rightarrow$ +ve

Electrolyte $\rightarrow$ Coating Obj. Sulphate Sol.

Different types of Secondary Cell, ElectricalNotebook.com

Sl. No.	Cell Name	+ve	-ve	Electrolyte	EMF	Internal R	η (Ah)	Wgt.
1.	Lead Acid Cell	PbO_2	Spongy Pb.	Dil. H_2SO_4	2.1V per Cell	Low	90-95%	Heavy
2.	Alkaline Cell (Ni-Fe Battery) (Edison cell)	$Ni(OH)_2$	Fe_2O_3 (In form of Fe_3O_4)	KOH	1.35V per Cell	High	80%	Light

Aircraft $\rightarrow$ Nickel-Iron (Ni-Fe) Battery.

Automobile $\rightarrow$ Lead Acid

Internal R of discharged battery is high.

L-A cell fully discharged $\rightarrow PbSO_4 \rightarrow$ Anode.

Float charging $\rightarrow$ Charge given to the battery when taken off the vehicle.

~~Carbon-Zn~~

Zn-C Cell $\rightarrow 1.5V$

Zn-Cl₂ Cell $\rightarrow 1.5V$

Mn-Alkaline Cell $\rightarrow 1.5V$

Silver Oxide Cell $\rightarrow 1.5V$ (Button size)

Lithium Cell $\rightarrow 2.95V$

Mercury Cell $\rightarrow 1.35V$